REMARKS

Claims remaining in the present patent application are Claims 1 – 20. Claims 1 – 9, 11 – 13 and 15 - 20 are amended herein. The Applicants note that no new matter has been introduced as a result of the claim amendments presented herein. The Applicants respectfully request consideration of the above captioned patent application in light of the claim amendments presented herein.

Attached hereto is a marked-up version of the changes made to the claims by the current amendments. The attachment is captioned "Version with Markings to Show Changes Made."

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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Date: 10/3/2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1 – 9, 11 – 13 and 15 - 20 have been amended as follows:

1. (Once Amended) A method for placing circuit elements on an integrated circuit comprising:

a) placing cells of a first circuit design by use of non-direct timing driven processes [techniques], wherein said placing produces a first placement; and

b) placing said cells by use of direct timing driven placement processes [techniques], wherein said first placement is an input into said b) placing.

2. (Once Amended) The method of Claim 1 wherein said a) comprises:

a1) placing cells of said [a] first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said a1) placing produces said [a] first placement.

3. (Once Amended) A method for placing circuit elements on an integrated circuit comprising:

a) placing cells of a first circuit design by use of non-direct timing driven processes [techniques], wherein said a) placing produces a first placement;

b) routing [said] wiring to connect said cells, wherein said routing produces a first layout;

c) modifying said first circuit design to produce second cells of a second circuit design; and

d) placing said second cells by use of direct timing driven placement processes [techniques].

4. (Once Amended) The method of Claim 3 wherein said a) comprises:

a1) placing cells of said [a] first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said a1) placing produces said [a] first placement.

5. (Once Amended) The method of Claim 3 wherein said b) comprises:

b1) estimating congestion for wiring to connect said cells, wherein said first placement is [further] said [a] first layout.

6. (Once Amended) The method of Claim 3 wherein said c) comprises:

c1) modifying said first circuit design to achieve minimum required signal timing within said first layout, wherein said modifying produces said [a] second circuit design containing second cells.

7. (Once Amended) The method of Claim 3 wherein said c) comprises:

c1) modifying said first circuit design to enlarge cell area allocations within congested regions of said first layout, wherein

said modifying produces said [a] second circuit design containing second cells.

8. (Once Amended) A method for placing circuit elements on an integrated circuit comprising:

a) placing cells of a first circuit design by use of non-direct timing driven processes [techniques], wherein said placing produces a first placement;

b) routing said wiring to connect said cells, wherein said routing produces a first layout;

c) placing said cells by use of direct timing driven placement processes [techniques] to produce a new placement, wherein said first layout is an input into said c) placing;

d) routing said new placement, wherein said d) routing produces a new layout; and

e) placing said cells by use of direct timing driven placement processes [techniques] to produce [still] another new placement, wherein said new layout is an input into said e) placing.

9. (Once Amended) The method of Claim 8 wherein said a) comprises:

a1) placing cells of said [a] first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said a1) placing produces said [a] first placement.

11. (Once Amended) The method of Claim 8 [wherein] further comprising repeating said d) and e)[are repeated].

12. (Once Amended) A method for placing circuit elements on an integrated circuit comprising:

a) synthesizing a high level description of a circuit to produce a first circuit design;

b) placing cells of said [a] first circuit design by use of non-direct timing driven processes [techniques], wherein said placing produces a first placement;

c) routing said wiring to connect said cells, wherein said routing produces a first layout;

d) modifying said first circuit design to produce a second high level description of a circuit;

e) synthesizing said second high level description of a circuit to produce a second circuit design; and

f) placing second cells of said second circuit design by use of direct timing driven placement processes [techniques].

13. (Once Amended) The method of Claim 12 wherein said b) comprises:

b1) placing cells of said [a] first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said b1) placing produces said [a] first placement.

15. The method of Claim 12 further comprising repeating [wherein] said c), e) and f)[are repeated].

16. (Once Amended) The method of Claim 12 further comprising repeating [wherein] said c), d), e) and f)[are repeated].

17. (Once Amended) The method of Claim 12 wherein said d) comprises:

d1) modifying said first circuit design to achieve minimum required signal timing within said first layout, wherein said d1) modifying produces said [a] second circuit design containing second cells.

18. (Once Amended) The method of Claim 12 wherein said d) comprises:

d1) modifying said first circuit design to enlarge cell area allocations within congested regions of said first layout, wherein said d1) modifying produces said [a] second circuit design containing second cells.

19. (Once Amended) A system comprising:

a processor coupled to a bus;

a memory coupled to said bus and wherein said memory contains instructions that when executed implement a method for placing circuit elements on an integrated circuit, said method comprising the steps of:

a) placing cells of a first circuit design without regard to circuit timing, wherein said placing produces a first placement; and

b) placing said cells by use of direct timing driven placement processes [techniques], wherein said first placement is an input into said placing.

20. (Once Amended) A system as described in Claim 19 wherein said a) comprises:

a1) placing cells of a first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said a1) placing produces said [a] first placement.